



# PCI-SIG ENGINEERING CHANGE NOTICE

<b>TITLE:</b>	1.8V sideband, Power Loss Notification, USB 2.0, and higher power support
<b>DATE:</b>	November 28, 2018
<b>AFFECTED DOCUMENT:</b>	PCIe M.2 Specification_Rev1.1 PCIe BGA SSD 11.5x13 ECN
<b>SPONSOR:</b>	Facebook, Intel, Micron, Sierra Wireless, Toshiba Memory Corp, WDC

## **Part I**

### **1. Summary of the Functional Changes**

This proposal introduces multiple features for M.2. These features include:

- Addition of 1.8V IO support type to Keys B, M, and B-M (1 pin)
- Addition of 1.8V IO Voltage source to Key M (1 pin)
- Addition of an optional pin for Power Loss Notification to Keys M, B-M, and BGA (1 pin)
- Addition of an optional pin for Power Loss Acknowledge to Keys B, M, B-M, and BGA (1 pin)
- Addition of an optional USB 2.0 interface to Key M (4 pins).
- Addition of an optional Power Disable pin for Key M (1 pin).
- Increase of static power to Key M and an addition of dynamic power including provisions to support for Keys B, M, and B-M.

The VIO 1.8 V signal is intended as an IO supply and reference voltage for host interface sideband signals PERST#, CLKREQ#, and PEWAKE# and additional signals such as SUSCLK, W\_DISABLE1#, PLN#, PWRDIS, and PLA\_S3#. This provides IO voltage flexibility to enable IO voltage levels other than 3.3V in the M.2 form factor. The use of the VIO 1.8 V supply is considered optional for Adapters that locally generate 1.8V from 3.3V for the host interface sideband signals.

The VIO\_CFG signal is intended to provide the Platform an indication of the IO voltage capabilities of the M.2 Adapter installed. In cases where the Platform detects that an incompatible Adapter is installed, the Platform may choose to not power the Adapter or isolate the affected sideband signals to avoid damage or interface instability.

The PLN signal is intended to trigger whatever power loss protection operation is appropriate for the PCIe function (e.g., SSD). The functionality of the power loss protection operation is expected to be developed in specifications related to the PCIe functionality (e.g., NVMe) and is not intended to interact with PCIe device or link power states. This functionality is optional.

The PLA signal is intended to signal to the Platform that the power loss protection operation has completed and that power may be safely removed.

The USB 2.0 interface is optional and intended to be used for debug or sideband communication.

The Power Disable pin is to notify the device that it shall be powered down.

The power increase support is optional as it is specific to the system implementation and power requirements of the device.

## **2. Benefits as a Result of the Changes**

Host Platform and M.2 Adapter logic may benefit from a transition to lower IO voltages as silicon processes transition to smaller process nodes. Smaller M.2 form factors may benefit from the resulting power reductions of a lower IO voltage.

Some use cases for the functions implemented in M.2 and BGA form factors would benefit from an out-of-band physical signal that triggers whatever power loss protection operation is appropriate for the PCIe function (e.g., SSD).

There is increased use of HW accelerators in computing. As a result, systems are adding the connectors to support however that means a dedicated connector for one usage only. There are additional usages that can be addressed and would benefit by adding a faster debug/sideband interface and defining the peak vs. normal power of M.2 for Sockets 2 and 3.

## **3. Assessment of the Impact**

This change updates the pin assignments and the socket current/power requirements for M.2 Sockets 2 and 3.

## **4. Analysis of the Hardware Implications**

This document defines usage of 3 pins for Socket 2 and 9 pins for Socket 3 that previous had no or optional functionality. 4 pins are defined to support a USB 2.0 interface along with ground shields that were previously no connects. One of the ground shields overlaps DEVSLP on the system which means the host will need to decide on USB 2.0 for sideband vs. DEVSLP for SATA support. 1 pin is defined to support the host telling the device to shut off any on-Adapter power rails. 1 pin is defined for voltage configuration of the Platform PCIe sidebands for 1.8V vs 3.3V which requires 3.3V tolerance for the Adapter. 1 pin is defined in Socket 3 as a IO power supply pin for 1.8V. Finally, this document defines 2 pins for power loss notification which communicate that a power loss event is happening along with an Adapter response.

## **5. Analysis of the Software Implications**

N/A.

## **6. Analysis of the C&I Test Implications**

N/A.

## Part II

# Changes to M.2 v1.1

<Editor's note: Existing M.2 v1.1 text is black. New text is marked in blue with underscore. Material to be deleted is ~~red with strikethrough~~.>

M.2 v1.1 Sections to be modified:

## 1.2. Targeted Application

The M.2 family of form factors is intended to support multiple function Adapter that include the following:

- ☐ Wi-Fi
- ☐ Bluetooth
- ☐ Global Navigation Satellite Systems (GNSS)
- ☐ Near Field Communication (NFC)
- ☐ WiGig
- ☐ WWAN (2G, 3G and 4G)
- ☐ Solid-State Storage Devices (SSD)
- ☐ Other and Future Solutions (e.g., Hybrid Digital Radio (HDR))
- ☐ Hardware Accelerator

## 2.4.3 System Connector Parametric Specifications

Table 13. Connector Electrical Requirements

Description	Requirement
Low Level Contact Resistance	EIA-364-23 <ul style="list-style-type: none"><li>• 55 mΩ maximum (initial) per contact</li><li>• 20 mΩ maximum change allowed</li></ul>
Insulation Resistance	EIA-364-21 <ul style="list-style-type: none"><li>• &gt;5 x 10<del>8</del><sup>8</sup> Ω @ 500 V DC</li></ul>
Dielectric Withstanding Voltage	EIA-364-20 <ul style="list-style-type: none"><li>• &gt;300 V AC (RMS) @ Sea Level</li></ul>
Current Rating	<ul style="list-style-type: none"><li>• 0.5 A/Power Contact (continuous), <u>1.0 A/Power contact (less than 100 us duration)</u></li><li>• The temperature rise above ambient must not exceed 30 °C.</li></ul>

Description	Requirement
	<ul style="list-style-type: none"> <li>The ambient condition is still air at 25 °C.</li> <li>EIA-364-70 Method 2</li> </ul>
Voltage Rating	50 V AC per Contact

## 3.2. WWAN/SSD/Other Socket 2 Adapter Interface Signals

Table 25. Socket 2 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Ground	3.3 V (5 pins)	I	3.3 V source	3.3 V
	VIO 1.8 V ( <a href="#">1 pin</a> )	I	I/O source (low current)	1.8 V ( <a href="#">Note 8</a> )
	GND (10+ pins)		Return current path.	0 V
Communication-specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the Platform chipset to reduce power and cost for the Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is $\pm 100$ ppm.	3.3 V <a href="#">1.8 V (Note 5)</a>
	W_DISABLE1#	I	Active low, debounced signal when applied by the system it will disable radio operation on the Adapters that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.	3.3 V <a href="#">1.8 V (Note 5)</a>
PCIe	PERST#	I	PCIe -Reset is a functional reset to the card as defined by the <i>PCI Express Mini CEM Specification</i> .	3.3 V (Note 3) 1.8 V (Note 4, <a href="#">5</a> )
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the <i>PCI Express Mini CEM Specification</i> . Open Drain with pull up on Platform. Active Low; also used by L1 PM Substates.	3.3 V (Note 3) 1.8 V (Note 4, <a href="#">5</a> )
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the Adapter supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	3.3 V (Note 3) 1.8 V (Note 4, <a href="#">5</a> )

<a href="#">Power Loss Signals</a>	<a href="#">PLN#</a>	<a href="#">I</a>	<a href="#">Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.</a>	<a href="#">3.3 V</a> <a href="#">1.8 V (Note 5, 6)</a>
	<a href="#">PLA_S2#</a>	<a href="#">O</a>	<a href="#">Power Loss Acknowledge. Active low signal with weak pull-down on Platforms that support power loss notification. An Adapter that supports this function must drive the signal to reflect its current power loss processing complete state.</a>	<a href="#">1.8 V (Note 5, 7)</a>
<a href="#">Optional Signals</a>	<a href="#">VIO_CFG</a>	<a href="#">O</a>	<a href="#">Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter.</a>	<a href="#">0 V/NC</a>

< Editor's Note: These footnotes attach to Table 25>

1. LED\_1# is valid for SSDs as well.
2. GPIO\_9 may be defined as LED\_1#, IPC\_7, or SATA DAS/DSS. Host systems should use the CONFIG pins (see 3.2.12), or other mechanisms, to ensure that these signals are fully electrically compatible, or that no electrically incompatible signals are driven onto these pins of an M.2 Adapter prior to discovery of the Adapter type.
3. Key B
4. Key C
5. [PCIe-based Key B and Key B-M Adapters when biased from a locally generated 1.8 V voltage on the Adapter. Adapters based on a locally generated 1.8 V must be 3.3 V tolerant for such sideband signaling. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters.](#)
6. [PLN# is valid for Socket 2 Key B-M PCIe-based SSD Adapters. Socket 2 Key B WWAN devices use FULL\\_CARD\\_POWER\\_OFF# instead.](#)
7. [Socket 2 PLA\\_S2# functionality differs from Socket 3 and BGA PLA\\_S3# functionality.](#)
8. [Required for PCIe-based Adapters that support 1.8V host interface sideband signaling that don't have a locally generated 1.8 V.](#)

### 3.2.11.3 General Purpose Input Output Pins

The GPIO\_0 to GPIO\_11 pins have configurable assignments. There are four possible functional pinouts configurations. These four configurations are called Port Config 0 to Port Config 3. In each Port Configuration, each GPIO is defined as a specific functional pin. The GPIO pin assignments are listed in Table 26.

Table 1. GPIO Pin Function Assignment per Port Configuration

	Pin	Port Config_0 (See Note 1)	Port Config_1 (See Note 2)	Port Config_2 (See Note 3)	Port Config_3 (See Note 3)	Note
<b>GPIO_0</b>	40	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0	
<b>GPIO_1</b>	42	GNSS_SDA	GNSS_SDA	UIM_DATA2	IPC_1	
<b>GPIO_2</b>	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2	
<b>GPIO_3</b>	46	SYSCLK	GNSS_0	UIM_RST2	IPC_3	
<b>GPIO_4</b>	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4	
<b>GPIO_5</b>	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0	
<b>GPIO_6</b>	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1	
<b>GPIO_7</b>	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2	
<b>GPIO_8</b>	28	AUDIO_3	AUDIO_3	<del>RFU</del> PLA_S2#	IPC_6/AUDIO_3	
<b>GPIO_9</b>	10	LED_1#	LED_1#	LED_1#	DAS/DSS/IPC_7	5, 6
<b>GPIO_10</b>	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE	
<b>GPIO_11</b>	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA	

#### Notes:

1. GNSS+Audio version 1
2. GNSS+Audio version 2
3. 2<sup>nd</sup> UIM/SIM Support
4. HSIC Support
5. Platform Providers may choose to implement IPC sideband instead of the LED\_1# to optimize their design
6. Some host Platforms (eg., tablets) may not require support for SSD. In such configurations, Host Platform Providers may choose to implement IPC\_7 on GPIO\_9 instead of DAS/DSS.

< Editor's Note: add after Section 3.2.14>

## 3.2.new Optional Signals

### 3.2.new.1 VIO CFG Signal

The VIO\_CFG (IO voltage configuration) is a signal that indicates to the Platform that the Adapter supports an independent IO voltage domain for the sideband signals. Adapters that use 3.3 V on sideband signals noted in Table 25 must connect VIO\_CFG directly to GND. Adapters that use 1.8

V sideband signaling (either through a voltage source on the Adapter or using the VIO 1.8 V pin) must not connect the VIO\_CFG pin and the affected signals on the Adapter must be 3.3 V tolerant. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters (e.g., prohibit applying power).



**Note:** A 3.3 V only sideband signaling Adapter as indicated when VIO\_CFG=GND is an indication that a 1.8 V only sideband signaling Platform should not attempt to utilize the Adapter. If an Adapter that supports 1.8 V sideband signaling as indicated by VIO\_CFG=NC on the Adapter is in a 3.3 V only Platform (i.e., VIO 1.8 V is not supplied) then the Adapter has the option to either not function or locally generate 1.8 V to configure itself and be 3.3V tolerant.

## 3.2.new2 Power Loss Signals

The Power Loss Signals are optional signals that are used to provide notification to an Adapter that a power loss event is expected to occur, and indicates the status of an Adapter's preparations for power loss.

### 3.2.new2.1 PLN# Signal

PLN# (Power Loss Notification) signal is an optional signal that informs an Adapter that a power loss event is expected to occur. If PLN# was asserted then is de-asserted before power is removed, the Adapter is permitted to return to normal operations. A Platform that supports this feature must assert PLN# prior to removing power from the Adapter. See 3.2.new2.3 for timing information.

Changes to the PCIe link activity due to PLN# assertion, or any functional response to this signal are outside the scope of this specification.

### 3.2.new2.2 PLA\_S2# Signal

The PLA\_S2# (Power Loss Acknowledge) signal is an optional signal under Port Config\_2 that indicates the status of an Adapter's preparations for a power loss. When implemented, Adapters that are powered on must actively drive PLA\_S2# regardless of the state of the PLN# signal. When implemented, Adapters always drive PLA\_S2# high (de-asserted) when not in power loss processing, and until drive it low (asserted) whenever power loss processing has completed. Implementations utilizing the optional PLN# signal (see 3.2.new2.1) should not require the optional PLA\_S2# signal to be implemented. See 3.2.new2.3 for timing information.

Any functional actions in response to this signal are outside the scope of this specification.



**Note:** Since power loss preparation takes time (and continued power) some Platform-specific mechanism such as a timer based delay can be used to control duration of power availability once PLN# is asserted. This shut down delay time may be minimized through the implementation of the PLA\_S2# signal.

### 3.2.new2.3 Timing Requirements for Power Loss Signals

Figure XX shows the sequencing behavior for the power loss signals. The minimum response time to a change in the PLN# or in the PLA\_S2# signal is 1.0  $\mu$ s. Any minimum assertion time or minimum negation time is outside the scope of this specification.

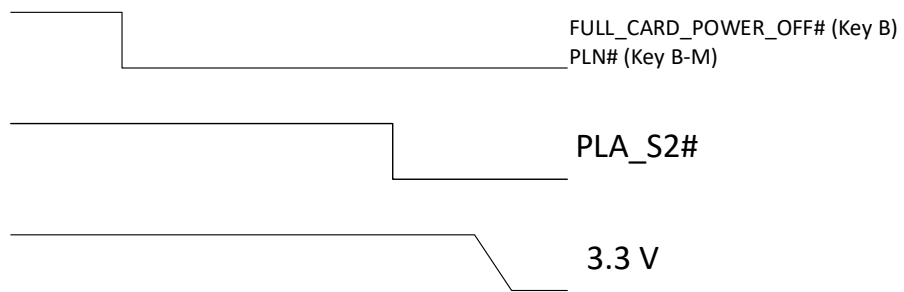


Figure xx. Power Loss Sequencing Behavior for Socket 2



Table 30. Socket 2 Key B SSIC-based WWAN Adapter Pinouts

< Editor's Note: Modified pins 8, 28, 68, and 73>

Pin	Signal	Signal	Pin
74	3.3 V	CONFIG_2 (States 8, 9, 10, 11)	75
72	3.3 V	<del>GND</del> VIO_CFG (O)	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	CONFIG_1 (States 8, 9, 10, 11)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	NC	ANTCTL0 (O)(0/1.8V)	59
56	NC	GND	57
54	NC	NC	55
52	NC	NC	53
50	NC	GND	51
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V)	NC	49
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V)	NC	47
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V)	GND	45
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V)	NC	43
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V)	NC	41
38	NC	GND	39
36	UIM_PWR (O)	SSIC-RxP	37
34	UIM_DATA (I/O)	SSIC-RxN	35
32	UIM_CLK (O)	GND	33
30	UIM_RESET (O)	SSIC-TxP	31
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	SSIC-TxN	29
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	GND	27
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	DPR (I)(0/1.8V)	25
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	CONFIG_0 = NC	21
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
		GND	11
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/1.8/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V or 3.3V)	GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3 = GND	1

**Table 31. Socket 2 Key B USB3.1 Gen1-based WWAN Adapter Pinout**

< Editor's Note: Modified pins 8, 28, 68, and 73 >

Pin	Signal	Signal	Pin
74	3.3 V	CONFIG_2 (States 4, 5, 6, 7)	75
72	3.3 V	<del>GND</del> VIO_CFG (O)	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	CONFIG_1 (States 4, 5, 6, 7)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	NC	ANTCTL0 (O)(0/1.8V)	59
56	NC	GND	57
54	NC	NC	55
52	NC	NC	53
50	NC	GND	51
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V)	NC	49
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V)	NC	47
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V)	GND	45
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V)	NC	43
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V)	NC	41
38	NC	GND	39
36	UIM-PWR (O)	USB3.0-Rx+	37
34	UIM-DATA (IO)	USB3.0-Rx-	35
32	UIM-CLK (O)	GND	33
30	UIM-RESET (O)	USB3.0-Tx+	31
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	USB3.0-Tx-	29
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	GND	27
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	DPR (I)(0/1.8V)	25
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	GPIO_11-WoWWAN#WoWWAN#WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	CONFIG_0 = GND	21
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	GND	11
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/1.8/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3 = NC	1

Table 32. Socket 2 Key B PCIe-based WWAN Adapter Pinout

< Editor's Note: Modified pins 73, 68, 54, 52, 50, 28, 8>

Pin	Signal	Signal	Pin
74	3.3 V	CONFIG_2 (States 2, 3, 12, 13)	75
72	3.3 V	<del>GND</del> VIO_CFG (O)	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	CONFIG_1 (States 2, 3, 12, 13)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	NC	ANTCTL0 (O)(0/1.8V)	59
56	NC	GND	57
54	PEWAKE# (I/O)(0/1.8/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/1.8/3.3V)	REFCLKn	53
50	PERST# (I)(0/1.8/3.3V)	GND	51
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERp0	49
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V*)	PERn0	47
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	GND	45
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V*)	PETp0	43
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V*)	PETn0	41
38	NC	GND	39
36	UIM-PWR (O)	PERp1	37
34	UIM-DATA (I/O)	PERn1	35
32	UIM-CLK (O)	GND	33
30	UIM-RESET (O)	PETp1	31
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	PETn1	29
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	GND	27
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	DPR (I)(0/1.8V)	25
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	CONFIG_0 (States 2, 3, 12, 13)	21
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
		GND	11
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/1.8/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)	GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3 (States 2, 3, 12, 13)	1

Table 2. Socket 2 Key B-M PCIe-based SSD Adapter Pinout

< Editor's Note: Modified pins 73, 68, 54, 52, 50, 28, and 8 >

Pin	Signal	Signal	Pin
74	3.3 V	CONFIG_2 = GND	75
72	3.3 V	<del>GND</del> VIO_CFG (O)	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	CONFIG_1 = NC	69
	ADD-IN CARD KEY M	NC	67
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/1.8/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/1.8/3.3V)	GND	51
50	PERST# (I)(0/1.8/3.3V)	PERp0	49
48	NC	PERn0	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	PETp0	43
42	SMB_DATA (I/O)(0/1.8V)	PETn0	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	NC	PERp1	37
36	NC	PERn1	35
34	NC	GND	33
32	NC	PETp1	31
30	NC	PETn1	29
28	<del>PLA_S2# (O)(0/1.8V)</del> NG	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	CONFIG_0 = GND	21
20	NC	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	LED_1#	NC	11
8	<del>PLN# (I) (0/1.8/3.3V)</del> NG	NC	9
6	NC	NC	7
4	3.3 V	NC	5
2	3.3 V	GND	3
		CONFIG_3 = GND	1

### 3.3. SSD Socket 3 Adapter Interface Signals

Table 36. Socket 3 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Ground	3.3 V (9 pins)	I	3.3 V source	3.3 V
	<a href="#">VIO 1.8 V (1 pin)</a>	<a href="#">I</a>	<a href="#">I/O source (low current)</a>	<a href="#">1.8 V (Note 1)</a>
	GND (154 pins)		Return current path.	0 V
PCIe	PERST#	I	PCIe Reference Clock signals (100 MHz) defined by the <i>PCI Express CEM Specification</i> .	3.3 V <a href="#">1.8 V (Note 2)</a>
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the <i>PCI Express Mini CEM Specification</i> ; Open Drain with pull up on Platform; Active Low; also used by L1 PM Substates.	3.3 V <a href="#">1.8 V (Note 2)</a>
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on Platform. Active Low when used as PEWAKE#. When the Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the Adapter supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	3.3 V <a href="#">1.8 V (Note 2)</a>
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the Platform chipset to reduce power and cost for the Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is $\pm 100$ ppm.	3.3 V <a href="#">1.8 V (Note 2)</a>
<a href="#">Optional Signals</a>	<a href="#">VIO_CFG</a>	<a href="#">O</a>	<a href="#">Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter.</a>	<a href="#">0 V/NC</a>
	<a href="#">PWRDIS</a>	<a href="#">I</a>	<a href="#">Active high with weak pull-down on Adapters. Power Disable notifies the Adapter to disable the power on the Adapter.</a>	<a href="#">3.3 V</a> <a href="#">1.8 V (Note 2)</a>
<a href="#">USB</a>	<a href="#">USB_D+</a> , <a href="#">USB_D-</a>	<a href="#">I/O</a>	<a href="#">USB Data <math>\pm</math> Differential serial data interface compliant to the <i>USB 2.0 Specification</i>.</a>	
<a href="#">Power Loss Signals (Note 3)</a>	<a href="#">PLN#</a>	<a href="#">I</a>	<a href="#">Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.</a>	<a href="#">3.3 V</a> <a href="#">1.8 V (Note 2)</a>

	<a href="#">PLA S3#</a>	<a href="#">O</a>	<a href="#">Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.</a>	<a href="#">3.3 V 1.8 V (Note 2, 4)</a>
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< Editor's Note: These footnotes attach to Table 36>

1. [Required for PCIe-based Adapters that support 1.8 V sideband signaling.](#)
2. [Must be 3.3 V tolerant for Adapters that support 1.8 V sideband signaling. See Section 3.3.new.1 for more details. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters.](#)
3. [Power Loss Signals PLN# and PLA S3# are valid for Socket 3 Key M PCIe-based SSD Adapters.](#)
4. [Note Socket 3 PLA S3# functionality differs from Socket 2 PLA S2# functionality. Socket 3 allows a host to tie together the PLA S3# signal such that the signal remains low until all connected Adapters have indicated completing power loss preparations by releasing PLA S3# \(i.e., wired-or functionality\)](#)

## 3.3.1 Power and Grounds

PCI Express M.2 Socket 3 utilizes a single 3.3 V power source similar to that of Socket 1 and 2. The voltage source, 3.3 V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In Socket 3, there is provision for nine 3.3 V pins to enable high continuous current, the same as in Socket 2 if required. The higher number of pins will help to reduce further the current resistance (IR) drop on the connector.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving GND pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

[The VIO 1.8 V power source is provided to supply the Adapter I/O buffer circuitry operating at 1.8 V sideband signaling. This power source is required for Adapters that support 1.8 V sideband signaling. Platforms that support 1.8 V sideband signaling must provide this power source. Adapters may provide 1.8 V sideband signaling based on the detection of this power source.](#)

< Editor's Note: Add after Section 3.3.4 >

## 3.3.new Optional Signals

### 3.3.new.1 VIO\_CFG Signal

[The VIO\\_CFG \(IO voltage configuration\) is a signal that indicates to the Platform that the Adapter supports an independent IO voltage domain for the sideband signals. Adapters that use 3.3 V on sideband signals noted in Table 36 must connect VIO\\_CFG directly to GND. Adapters that use 1.8](#)

V sideband signaling (either through a voltage source on the Adapter or using the VIO 1.8 V pin) must not connect the VIO\_CFG pin and the affected signals on the Adapter must be 3.3 V tolerant. Platforms that expect 1.8 V sideband signaling must protect themselves from legacy 3.3 V adapters (e.g., prohibit applying power).



**Note:** A 3.3 V only sideband signaling Adapter as indicated when VIO\_CFG=GND is an indication that a 1.8 V only sideband signaling Platform should not attempt to utilize the Adapter. If an Adapter that supports 1.8 V sideband signaling as indicated by VIO\_CFG=NC on the Adapter is in a 3.3 V only Platform (i.e., VIO 1.8 V is not supplied) then the Adapter has the option to either not function or locally generate 1.8 V to configure itself and be 3.3V tolerant.

## 3.3.new.2 PWRDIS

The Power Disable (PWRDIS) signal is an optional signal used to disable the power on the M.2 Adapter. When this signal is asserted, the Adapter shall disable the power to the circuits on the Adapter. The PCIe link may not be functional during this time. The host may provide power when PWRDIS is asserted. When this signal is de-asserted the Adapter shall allow power to the circuits on the Adapter.

The Power Disable (PWRDIS) AC characteristics are provided in Table xx

Table xx. PWRDIS AC characteristics

<u>Parameter</u>	<u>Min</u>	<u>Max</u>	<u>Unit</u>
<u>PWRDIS asserted hold time</u>		<u>5</u>	<u>s</u>
<u>PWRDIS de-asserted hold time</u>		<u>0.1</u>	<u>s</u>
<b>Note:</b> The hold time is the length of time PWRDIS is asserted or de-asserted. This timing shall include time of 1 us to recognize a change on PWRDIS (de-bounce time).			

## 3.3.new2. USB Interface

See Section 3.1.5 for a detailed description of the USB signals.

## 3.3.new3. Power Loss Signals

The Power Loss Signals are optional signals that are used to provide notification to an Adapter that a power loss event is expected to occur, and indicates the status of an Adapter's preparations for power loss.

### 3.3.new3.1 PLN# Signal

See Section 3.2.new2.1 for a more detailed description of PLN# and Section 3.3.new3.3 for timing information.

### 3.3.new3.2 PLA\_S3# Signal

The PLA\_S3# (Power Loss Acknowledge) signal is an optional signal that indicates the status of an Adapter's preparations for a power loss. The open-drain requirement on the Adapter allows a host to tie together the PLA\_S3# signal from multiple Adapters such that the signal remains low (asserted) until all connected Adapters have completed power loss preparation (i.e., wired-or functionality). Implementations utilizing the optional PLN# signal (see 3.3.new3.1) should not require the optional PLA\_S3# signal to be implemented. See 3.3.new3.3 for timing information. Any functional actions in response to this signal are outside the scope of this specification.



**Note:** Since power loss preparation takes time (and continued power) some Platform-specific mechanism such as a timer based delay can be used to control duration of power availability once PLN# is asserted. This shut down delay time may be minimized through the implementation of the PLA\_S3# signal.

### 3.3.new3.3 Timing Requirements for Power Loss Signals

Figure XX shows the sequencing behavior for the power loss signals. The minimum response time to a change in the PLN# or in the PLA\_S3# signal is 1.0  $\mu$ s. Any minimum assertion time or minimum negation time is outside the scope of this specification.

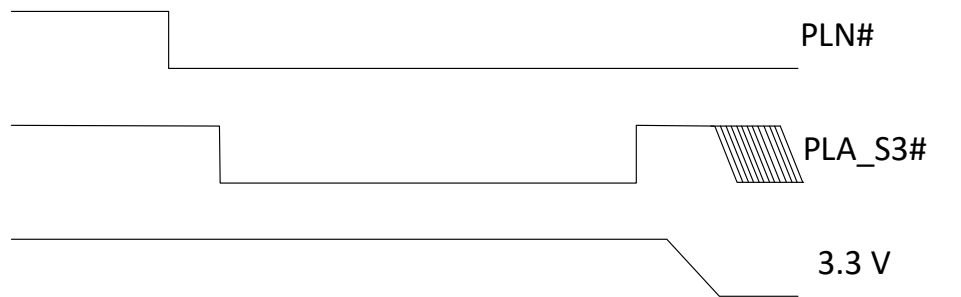


Figure xx. Power Loss Sequencing Behavior for Socket 3

### 3.3.5. Socket 3 Connector Pinout Definitions



All pinouts tables in this section are written from the Adapter point of view when referencing signal directions.

Table 37 and Table 38 list the signal pinouts for the Add-in Card edge card connector. Table 37 lists the SATA based solution pinouts. Table 38 lists the PCIe Multi-lane based solution pinouts.



Table 38. Socket 3 PCIe-based Adapter Pinouts (Key M)

< Editor's Note: changed pins 73, 54, 52, 50, 38, 36, 34, 32, 30, 22, 8, and 6 >

Pin	Signal	Signal	Pin
74	3.3V	GND	75
72	3.3V	<del>GND</del> VIO_CFG (O)	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/1.8/3.3V)	PEDET (NC-PCIe)	69
	ADD_IN CARD KEY M	NC	67
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
	ADD_IN CARD KEY M	ADD_IN CARD KEY M	
58	Reserved for MFG_CLOCK	ADD_IN CARD KEY M	
56	Reserved for MFG_DATA	GND	57
54	PEWAKE# (I/O)(0/1.8/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/1.8/3.3V)	REFCLKn	53
50	PERST# (I)(0/1.8/3.3V)	GND	51
48	NC	PERp0	49
46	NC	PERn0	47
44	ALERT# (O)(0/1.8V)	GND	45
42	SMB_DATA (I/O)(0/1.8V)	PETp0	43
40	SMB_CLK (I/O)(0/1.8V)	PETn0	41
38	<del>GND</del> NC	GND	39
36	<del>USB_D</del> NC	PERp1	37
34	<del>USB_D+</del> NC	PERn1	35
32	<del>GND</del> NC	GND	33
30	<del>PLA_S3# (O)(0/1.8/3.3V)</del> NC	PETp1	31
28	NC	PETn1	29
26	NC	GND	27
24	NC	PERp2	25
22	<del>VIO 1.8 V</del> NC	PERn2	23
20	NC	GND	21
18	3.3V	PETp2	19
16	3.3V	PETn2	17
14	3.3V	GND	15
12	3.3V	PERp3	13
10	LED_1# (O)	PERn3	11
8	<del>PLN# (I) (0/1.8/3.3V)</del> NC	GND	9
6	<del>PWRDIS (I) (0/1.8/3.3V)</del> NC	PETp3	7
4	3.3V	PETn3	5
2	3.3V	GND	3
		GND	1

## 3.4. BGA SSD Interface Signals

Table 39. BGA SSD System Interface Signal Table

< Editor's Note: At end of table>

Interface	Signal Name	I/O	Function	Voltage
<a href="#">Power Loss Signals</a>	<a href="#">PLN#</a>	<a href="#">I</a>	<a href="#">Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.</a>	<a href="#">1.8 V</a>
	<a href="#">PLA S3#</a>	<a href="#">O</a>	<a href="#">Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.</a>	<a href="#">1.8 V</a>

< Editor's Note: Add after Section 3.4.5.7>

### 3.4.new Power Loss Signals

[The Power Loss Signals are optional signals that are used to provide notification to an Adapter that a power loss event is expected to occur, and indicates the status of an Adapter's preparations for power loss.](#)

#### 3.4.new.1 PLN# Signal

[See Section 3.2.new2.1 for a more detailed description of PLN# and Section 3.3.new3.3 for timing information.](#)

#### 3.4.new.2 PLA S3# Signal

[See Section 3.3.new3.2 for a more detailed description of PLA S3#.](#)

<Editor's Note: In Figure 104 replace text and change color to dark green in cells:

H15: PLN#~~RFU~~

K15: PLA\_S3#~~RFU~~>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNV	DNV		DNV		DNV		DNV			DNV		DNV		DNV		DNV	DNV
B	DNV	DNV		DNV		CAL_P		DNV			DNV		DNV		DNV		DNV	DNV
C	GND	GND	GND	GND	GND	DNV	XTAL_OUT	XTAL_IN	DNV	RZQ_1	DNV	DNV	RFU	RFU	GND	DNV	DNV	DNV
D				REFCLKp	REFCLKn	GND	PERSt#	CLKREQ#	3.3 V	3.3 V	GND	DNV	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3 V	3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNV	DNV	DNV
F				SATA-A- / PERp0	SATA-A- / PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNV	DNV	DNV
H				SATA-B- / PETp0	SATA-B- / PETn0		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNV	DNV	DNV
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNV	DNV	JTAG_TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNV	JTAG_TCK	JTAG_TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNV	JTAG_TDI	JTAG_TDO
T				PETp2	PETn2		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNV	SMB_CLK	SMB_DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1# / DAS	RFU	3.3 V	3.3 V	GND	RFU	RFU	GND	GND	DNV	DNV	ALERT#
Y				PETp3	PETn3	GND	DNV	DNV	3.3 V	3.3 V	GND	DNV	GND	DNV	DNV			
AA	GND	GND	GND	GND	GND	DNV	DNV	DNV	DNV	RZQ_2	DNV	DNV	DNV	GND	GND	DNV	DNV	DNV
AB	DNV	DNV		DNV		DNV		DNV			DNV		DNV		DNV		DNV	DNV
AC	DNV	DNV		DNV		DNV		DNV			DNV		DNV		DNV		DNV	DNV


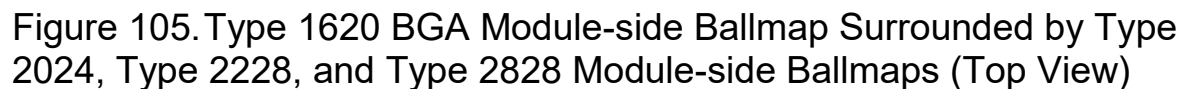
 = No Solder Ball

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

K15: PLA S3#~~RFU~~>



## 4.2. 1.8 V Logic Signal Requirements

The 1.8 V card logic levels for single-ended digital signals ([PCIe sideband](#), SDIO, UART, I2C, PCM/I2S, SMBus, [PWRDIS](#), [PLN#](#), [PLA S2#](#), [PLA S3#](#), etc.) are given in Table 41. This table also defines the signaling levels for BGA SSD defined single-ended signals such as (PERST#, CLKREQ#, PEWAKE#, SUSCLK, SMB\_CLK, SMB\_DAT, ALERT#, [PLN#](#), [PLA S3#](#)).

<Editor's Note: Add after Section 4.2>

## 4.new. Electrical Requirements for M.2 Adapters

### 4.new.1. Voltage Supply Power-on Sequencing

It is recommended that the host should apply the following power rail sequencing for Platforms that implement the VIO 1.8 V supply. During power-on:

- ❑ After the voltage on either the 3.3 V supply or the voltage on the VIO 1.8 V supply reach 300 mV, the voltage on the 3.3 V supply should remain greater than the VIO 1.8 V by at least 200 mV.

If the power-on sequencing is not followed, there is a risk that the Adapter may not power-on correctly or the Adapter may be damaged. These results are vendor specific.

### 4.new.2. Voltage Supply Power-off Sequencing

It is recommended that the host should apply the following power rail sequencing for Platforms that implement the VIO 1.8 V supply. During power-off:

- ❑ Before the voltage on both the 3.3 V supply and the VIO 1.8 V supply drops below 300 mV, the voltage on the 3.3 V supply should remain greater than voltage on the VIO 1.8 V supply by 200 mV.
- ❑ After the voltage on both the 3.3 V supply and the VIO 1.8 V supply are below 300 mV, there is no specified relationship between them.
- ❑ The voltage on all supplies should remain below 100 mV for at least 1 ms before the power-on sequence is attempted.

If the power-off sequencing is not followed, there is a risk that the Adapter may not power-off correctly or the Adapter may be damaged. These results are vendor specific.

<Editor's Note: Sections 4.3 and 4.4 renumbered based on above section insertion>

## 4.4. Power

The M.2 Adapter utilizes a single regulated power rail of 3.3 V provided by the Platform. In some pinout Adapter, there is a dedicated VIO supply pin called [VIO 1.8 V](#) that is intended to bias the I/O circuitry of the Adapter. [Signals that are powered by VIO 1.8 V in Key M PCIe-based Adapters or by an internal voltage source for Key B and Key B-M specifically must be 3.3 V tolerant in the event that VIO 1.8 V is not provided by the Platform.](#) The main 3.3 V and the VIO voltage rail sources on the Platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card. Some NICs require host (driver) intervention after a power-on.

The number of 3.3 V pins for any given pinout is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2 connector current handling capability per pin. The M.2 connector pin is defined as needing to support 500 mA/pin continuous. This yields the required number of power rail pins per pinout.

- ❑ Type 1630, intended for Socket 1, has two power pins allocated in the pinouts that supports up to 1 A continuous.
- ❑ Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and support up to 2 A continuous.
- ❑ The Socket 2 board types have five power pins in their pinouts and support up to 2.5 A continuous. [To improve current balancing between power pins, it is recommended that the resistance delta due to trace lengths/widths between any 3.3 V pin be designed to be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.](#)
- ❑ The Socket 3 board types, with a single Add-in Card Key, have nine power pins but support up to ~~2.5~~3.5 A continuous. [Continuous current requires sufficient power dissipation capability \(e.g. airflow, heat sink, etc.\). This capability is outside the scope of this specification. To improve current balancing between power pins, it is recommended that the resistance delta due to trace lengths/widths between any 3.3 V pin be designed to be less than 15 mΩ on the Platform and less than 15 mΩ on the Adapter.](#)
- ❑ The ~~four~~ extra power pins, [beyond the number of pins that support the continuous current](#), enable reduced IR drop for these devices.

Table 46. Power Rating Table for M.2 Modules with Connectors

Key	Power Rail	Voltage Tolerance	Current Consumption Limit	
			Peak <sup>1</sup> mA Max Avg @ 100 $\mu$ s	Normal <sup>2</sup> mA Max Avg @ 1 s
A	3.3 V	$\pm 5\%$	2000	
<del>B</del>	<del>3.3 V</del>	<del><math>\pm 5\%</math></del>	<del>2500</del>	
<u>B</u>	<u>3.3 V</u>	<u><math>\pm 5\%</math></u>	<u>5000<sup>6</sup></u>	<u>2500<sup>5</sup></u>
B	V <sub>BAT</sub>	3.135 V – 4.4 V	2500	
C	3.3 V	$\pm 5\%$	2500	
C	V <sub>BAT</sub>	3.135 V – 4.4 V	2500	
C	1.8 V <sup>3</sup>	$\pm 5.55\%^4$	70	
D	RFU	RFU	RFU	RFU
E	3.3 V	$\pm 5\%$	2000	
F	RFU	RFU	RFU	RFU
G	N/A	N/A	N/A	N/A
H	RFU	RFU	RFU	RFU
J	RFU	RFU	RFU	RFU
K	RFU	RFU	RFU	RFU
L	RFU	RFU	RFU	RFU
<del>M</del>	<del>3.3 V</del>	<del><math>\pm 5\%</math></del>	<del>2500</del>	
<u>M</u>	<u>3.3 V</u>	<u><math>\pm 5\%</math></u>	<u>7000<sup>6</sup></u>	<u>3500<sup>5</sup></u>
<u>M</u>	<u>1.8 V<sup>3</sup></u>	<u><math>\pm 5.55\%^4</math></u>	<u>70</u>	

<sup>1</sup> Peak is ~~is not~~ the maximum highest averaged current value over any 100  $\mu$ s period

<sup>2</sup> Normal is ~~is not~~ the maximum highest averaged current value over any 1 s period

<sup>3</sup> Pin name VIO 1.8 V

<sup>4</sup> 1.7 V to 1.9 V Range

<sup>5</sup> Normal currents assume sufficient power dissipation capability by the Platform. This capability is outside the scope of this specification. The maximum power of device may be controlled through function specific capabilities (e.g., for SSDs see NVMe).

<sup>6</sup> The peak current's duty cycle shall ensure that the normal current is not violated.

### 5.2.1.2. Socket 2 Pinout (Mechanical Key B) On Platform

Table 52. Socket 2 Pinouts Diagram (Mechanical Key B) On Platform

< Editor's Note: changed pins 8, 28, 50, 52, 54, 68, and 73>

74	3.3 V	CONFIG_2	75
72	3.3 V	<a href="#">VIO_CFG (I) or</a> GND	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (O)(0/1.8/3.3V)	CONFIG_1	69
66	SIM DETECT (O)	RESET# (O)(0/1.8V)	67
64	COEX_RXD (I)(0/1.8V)	ANTCTL3 (I)(0/1.8V)	65
62	COEX_TXD (O)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
58	NC	ANTCTL0 (I)(0/1.8V)	59
56	NC	GND	57
54	PEWAKE# (I/O)(0/1.8/3.3V)	REFCLKp	55
52	CLKREQ# (I/O)(0/1.8/3.3V)	REFCLKn	53
50	PERST# (O)(0/1.8/3.3V)	GND	51
48	GPIO_4 (I/O)(0/1.8V)	PETp0/SATA-A+	49
46	GPIO_3 (I/O)(0/1.8V)	PETn0/SATA-A-	47
44	GPIO_2 (I/O)/ALERT# (I)(0/1.8V)	GND	45
42	GPIO_1 (I/O)/SMB_DATA (I/O)(0/1.8V)	PERp0/SATA-B-	43
40	GPIO_0 (I/O)/SMB_CLK (I/O)(0/1.8V)	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	UIM-PWR (I)	PETp1/USB3.0-Tx+/SSIC-TxP	37
34	UIM-DATA (I/O)	PETn1/USB3.0-Tx-/SSIC-TxN	35
32	UIM-CLK (I)	GND	33
30	UIM-RESET (I)	PERp1/USB3.0-Rx+/SSIC-RxP	31
28	<a href="#">PLA_S2# (I)/GPIO_8 (I/O) (0/1.8V)</a>	PERn1/USB3.0-Rx-/SSIC-RxN	29
26	GPIO_10 (I/O) (0/1.8V)	GND	27
24	GPIO_7 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
22	GPIO_6 (I/O)(0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
20	GPIO_5 (I/O)(0/1.8V)	CONFIG_0	21
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
10	GPIO_9/DAS/DSS# (I/O)/LED_1# (I)(0/3.3V)	GND	11
8	W_DISABLE1# (O)(0/1.8/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (O) (0/1.8V or 3.3V)	USB_D+	7
4	3.3 V	GND	5
		GND	3
2	3.3 V	CONFIG_3	1



## 5.3. SSD Socket; Socket 3 (Mechanical Key M)

< Editor's Note: changed pins 6, 8, 22, 30, 32, 34, 36, 38, 50, 52, 54, 68, and 73>

Table 54. Socket 3 SSD Pinout (Mechanical Key M) On Platform

74	3.3 V	GND	75
72	3.3 V	<a href="#">VIO_CFG (I) or GND</a>	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (O)(0/1.8/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	CONNECTOR KEY M	NC	67
	CONNECTOR KEY M	CONNECTOR KEY M	
	CONNECTOR KEY M	CONNECTOR KEY M	
	CONNECTOR KEY M	CONNECTOR KEY M	
58	NC	CONNECTOR KEY M	
56	NC	GND	57
54	PEWAKE# (I/O)(0/1.8/3.3V) or NC	REFCLKp	55
52	CLKREQ# (I/O)(0/1.8/3.3V) or NC	REFCLKn	53
50	PERST# (O)(0/1.8/3.3V) or NC	GND	51
48	NC	PETp0/SATA-A+	49
46	NC	PETn0/SATA-A-	47
44	ALERT# (I) (0/1.8V)	GND	45
42	SMB_DATA (I/O) (0/1.8V)	PERp0/SATA-B-	43
40	SMB_CLK (I/O)(0/1.8V)	PERn0/SATA-B+	41
38	DEVSLP (O) <a href="#">(SATA) or GND (USB)</a>	GND	39
36	<a href="#">USB_D- or NC</a>	PETp1	37
34	<a href="#">USB_D+ or NC</a>	PETn1	35
32	<a href="#">NC or GND (USB)</a>	GND	33
30	<a href="#">PLA_S3# (I)(0/3.3V) or NC</a>	PERp1	31
28	NC	PERn1	29
26	NC	GND	27
24	NC	PETp2	25
22	<a href="#">VIO 1.8 V or NC</a>	PETn2	23
20	NC	GND	21
18	3.3 V	PERp2	19
16	3.3 V	PERn2	17
14	3.3 V	GND	15
12	3.3 V	PETp3	13
10	DAS/DSS# (I/O)/LED_1# (I)(0/3.3V)	PETn3	11
8	<a href="#">PLN# (O) (0/1.8/3.3V) or NC</a>	GND	9
6	<a href="#">PWRDIS (O)(0/1.8/3.3V) or NC</a>	PERp3	7
4	3.3 V	PERn3	5
2	3.3 V	GND	3
		GND	1

Although the pinouts in Table 54 allocates four additional 3.3 V power pins, it is not intended to increase the current sinking capability of the Adapter without sufficient power dissipation capability from the Platform. This capability is outside the scope of this specification. The intention is to further reduce the IR drop of the power under extreme high current cases and increase the robustness of the SSD devices. For higher power applications, the resistance between any two 3.3 V pins on the host and device shall be less than 15 mΩ. The maximum power consumption of this socket remains as identified in section 3.3, *SSD Socket 3 System Interface Signals*. This socket will also accept SSD devices Add-in Cards that employ a Dual Module key on Module scheme. The SMBus interface available on Socket 3 is used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.

If Platform provides USB D+/USB D- (pins 34 and 26), then ground pins at pin 30 and pin 38 are must be used.

## 5.4. Soldered Down Pinouts Definitions

<Editor's Note: In Figure 111 replace text and change color to dark green in cells:

H15: PLN#~~RFU~~

K15: PLA\_S3#~~RFU~~>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNV	DNV		DNV		DNV		DNV			DNV		DNV		DNV		DNV	DNV
B	DNV	DNV		DNV		CAL_P		DNV			DNV		DNV		DNV		DNV	DNV
C	GND	GND	GND	GND	GND	DNV	XTAL_OUT	XTAL_IN	DNV	R2D_1	DNV	DNV	RFU	RFU	GND	DNV	DNV	DNV
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	+3.3 V	+3.3 V	GND	DNV	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVBLP	+3.3 V	+3.3 V	GND	PERMRES	DIAG0	GND	GND	DNV	DNV	DNV
F				SATA-B+/PETp0	SATA-B-/PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNV	DNV	DNV
H				SATA-B+/PERp0	SATA-B-/PERn0		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNV	DNV	DNV
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNV	DNV	JTAG_TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNV	JTAG_TCK	JTAG_TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNV	JTAG_TDI	JTAG_TDO
T				PERp2	PERn2		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNV	SMC_CLK	SMC_DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1H/DAS	RFU	+3.3 V	+3.3 V	GND	RFU	RFU	GND	GND	DNV	DNV	ALERT#
Y				PERp3	PERn3	GND	DNV	DNV	+3.3 V	+3.3 V	GND	DNV	GND	DNV	DNV			
AA	GND	GND	GND	GND	GND	DNV	DNV	DNV	DNV	R2D_2	DNV	DNV	DNV	GND	GND	DNV	DNV	DNV
AB	DNV	DNV		DNV		DNV		DNV			DNV		DNV		DNV		DNV	DNV
AC	DNV	DNV		DNV		DNV		DNV			DNV		DNV		DNV		DNV	DNV

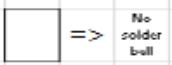


Figure 111. Type 1620 BGA Pinout On Platform (Top View)

<Editor's Note: In Figure 112 replace text and change color to dark green in cells (using Type 1620 naming grid):

H15: PLN#~~RFU~~

K15: PLA S3#~~RFU~~>

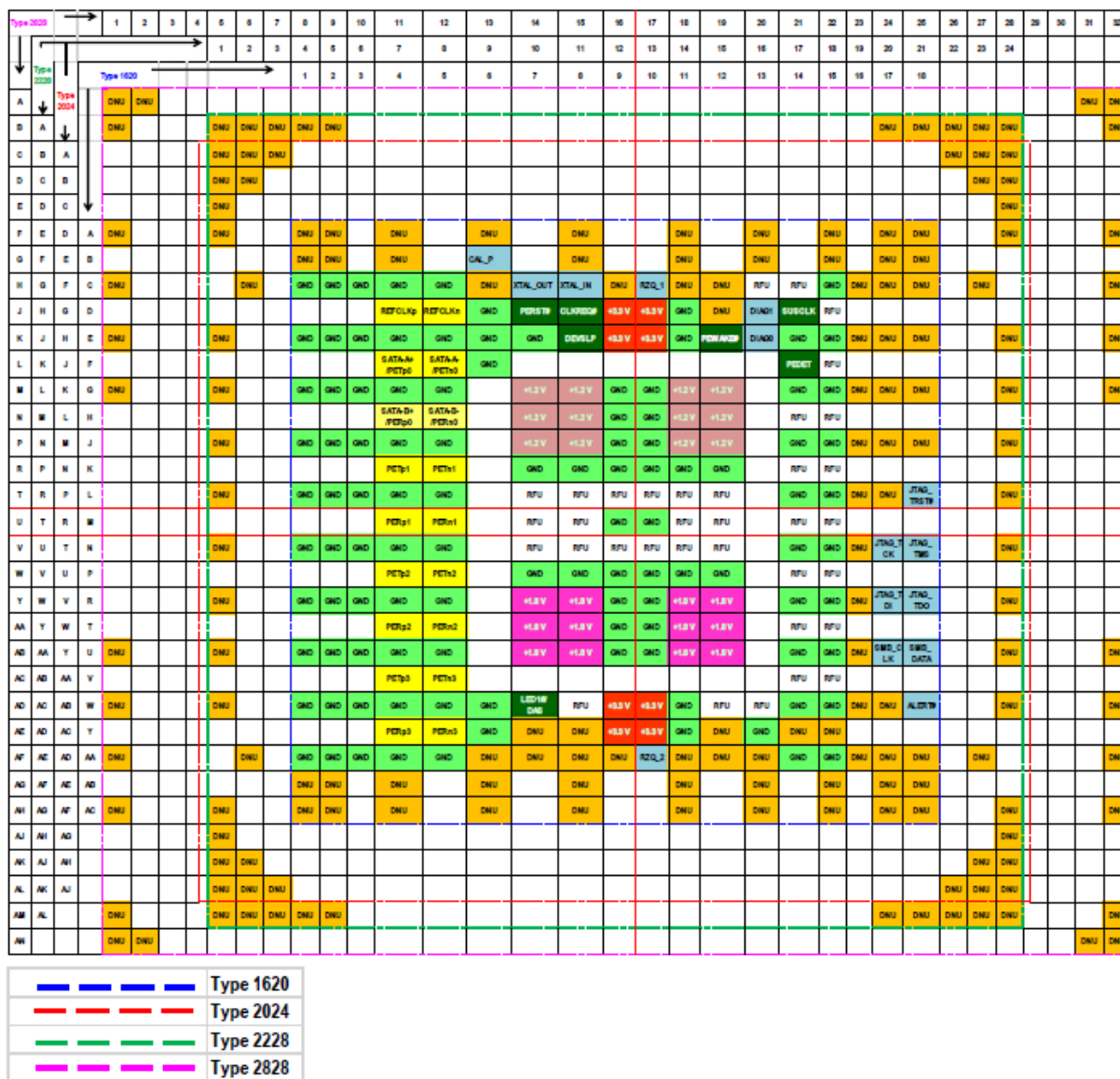


Figure 112. Type 1620, Type 2024, Type 2228, Type 2828 BGA Pinout On Platform (Top View)

## Part III

# Changes to PCIe BGA SSD 11.5x13 ECN.

<Editor's note: Existing PCIe BGA SSD 11.5x13 ECN text is black. New text is marked in blue with underscore. Material to be deleted ~~is red with strikethrough.~~>

## 3.4 BGA SSD Interface Signals

<Table <Editor's Note: R12g is confused here – table labels belong before the table>

Table 39. BGA SSD System Interface Signal Table for Types 1620, 2024, 2228, and 2828

Interface	Signal Name	I/O	Function	Voltage
<u>Power Loss Signals</u>	<u>PLN#</u>	<u>I</u>	<u>Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.</u>	<u>PWR_2</u>
	<u>PLA_S3#</u>	<u>O</u>	<u>Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.</u>	<u>PWR_2</u>

Table 39a. BGA SSD System Interface Signal Table for Type 1113

Interface	Signal Name	I/O	Function	Voltage
<u>Power Loss Signals</u>	<u>PLN#</u>	<u>I</u>	<u>Power Loss Notification. Open drain with a pull-up on Adapters that support power loss notification. When the Platform supports power loss notification, this signal is asserted to indicate a power loss event is expected to occur. When the Adapter supports this function and the signal is asserted then it must ready itself for power loss.</u>	<u>PWR_2</u>

	<a href="#">PLA S3#</a>	<a href="#">O</a>	<a href="#">Power Loss Acknowledge. Open drain with pull-up on Platforms that support power loss notification. An Adapter that supports this function, must drive the signal to reflect its current power loss processing complete state.</a>	<a href="#">PWR 2</a>
--	-------------------------	-------------------	---	-----------------------

<Editor's Note 3.4.new is the same as in the ECR for M.2 1.1>

## **3.4.new Power Loss Signals**

The Power Loss Signals are optional signals that are used to provide notification to an Adapter that a power loss event is expected to occur, and indicates the status of an Adapter's preparations for power loss.

### **3.4.new.1 PLN# Signal**

See Section 3.2.new2.1 for a more detailed description of PLN# and Section 3.3.new3.3 for timing information.

### **3.4.new.2 PLA S3# Signal**

See Section 3.3.new3.2 for a more detailed description of PLA S3#.

### 3.4.6. BGA SSD Soldered-Down Module Pin-out

<Editor's Note: Duplicate and Identical to changes made earlier in this document.

In Figure 104 replace text and change color to dark green in cells:

H15: ~~PLN#~~RFU

K15: ~~PLA S3#~~RFU>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	R2Q_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3V PWR_1	3.3V PWR_1	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3V PWR_1	3.3V PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- / PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		1.2V PWR_3	1.2V PWR_3	GND	GND	1.2V PWR_3	1.2V PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+ / PETp0	SATA-B- / PETn0		1.2V PWR_3	1.2V PWR_3	GND	GND	1.2V PWR_3	1.2V PWR_3		RFU	RFU			
J	GND	GND	GND	GND	GND		1.2V PWR_3	1.2V PWR_3	GND	GND	1.2V PWR_3	1.2V PWR_3		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		1.8V PWR_2	1.8V PWR_2	GND	GND	1.8V PWR_2	1.8V PWR_2		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PETp2	PETn2		1.8V PWR_2	1.8V PWR_2	GND	GND	1.8V PWR_2	1.8V PWR_2		RFU	RFU			
U	GND	GND	GND	GND	GND		1.8V PWR_2	1.8V PWR_2	GND	GND	1.8V PWR_2	1.8V PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED_1# / DAS	RFU	3.3V PWR_1	3.3V PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	3.3V PWR_1	3.3V PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	R2Q_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

<Editor's Note: In Figure 105 replace text and change color to dark green in cells (using Type 1620 naming grid):

H15: PLN#RFU

K15: PLA S3#RFU>

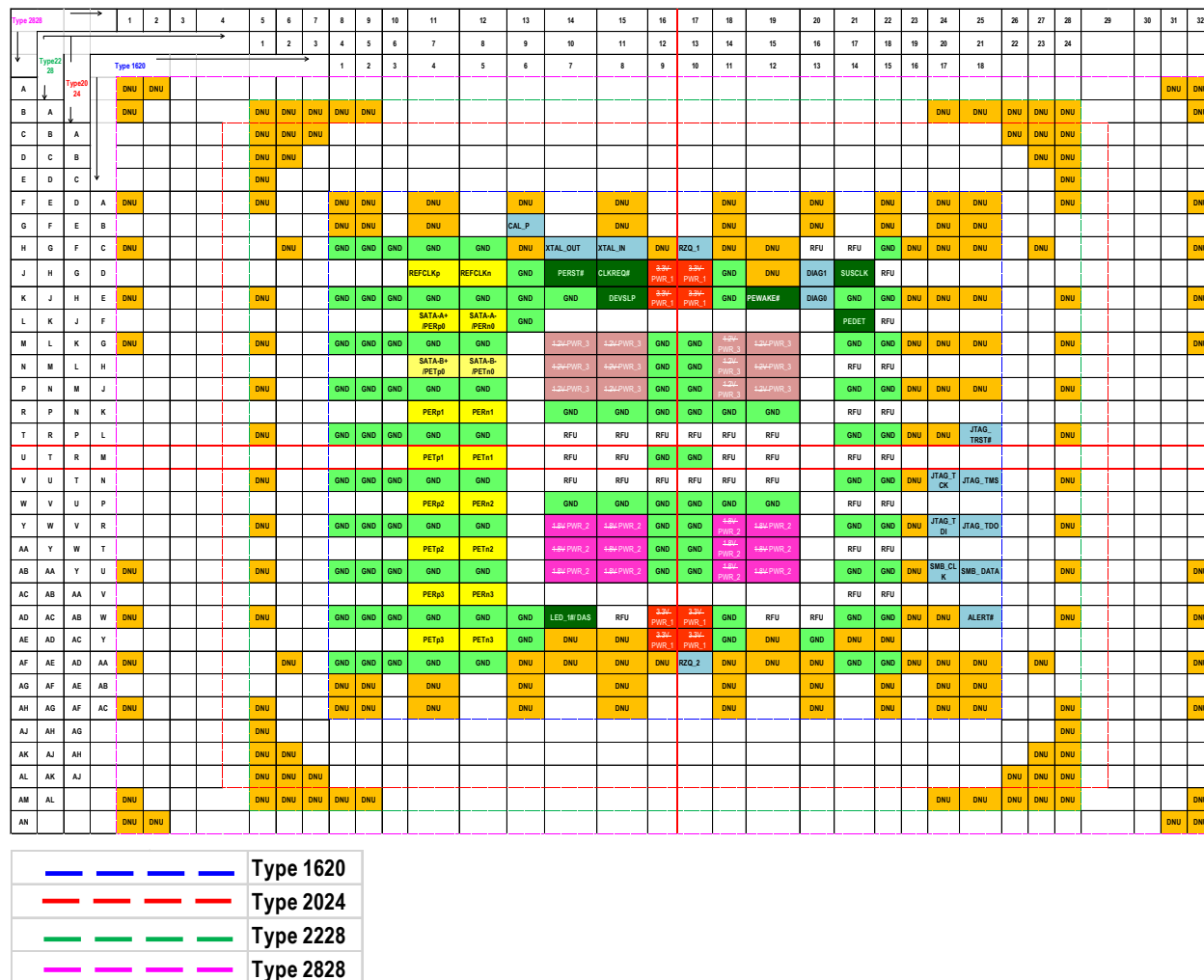


Figure 105. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)



<Editor's Note: In Figure 105a replace text and change color to dark green in cells:

C10: PLN#~~RFU~~

D10: PLA\_S3#~~RFU~~>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REQ_D1	REQ_D2	REQ_D3			GND			GND			GND	WP_L	SPI_CLK	SPI_CS_L	GND	GND
C	GND	GND	GND	DNV	DNV	RFU	RFU	RFU	RFU	RFU	SMB_DAT_A	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPI_MOSI	SPI_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNV	DNV	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPI_SS	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	GND	PWR_2	PWR_2	
G		GND	GND	GND	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	GND	GND	
H	GND	PWR_1	PWR_1	H3B	H3B	H3B	H3B								H3B	H3B	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	H3B	H3B		H3B	H3B	H3B	H3B	H3B	H3B		H3B	H3B	H3B	PWR_1	PWR_1	
K		GND	PWR_1	H3B	H3B	H3B		H3B							H3B	H3B	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	H3B	H3B		H3B							H3B	H3B	H3B	GND	RZQ_2	GND
M	GND	GND	PWR_3	H3B	H3B	H3B		H3B							H3B	H3B	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	H3B	H3B		H3B							H3B	H3B	H3B	PWR_3	PWR_3	
P		PWR_3	PWR_3	H3B	H3B	H3B		H3B	H3B	H3B	H3B	H3B	H3B		H3B	H3B	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	H3B	H3B									H3B	H3B	H3B	GND	GND	GND
T		PWR_2	PWR_2	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	H3B	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PER07#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	GND	LED_1#	GND	GND	GND	GND	PER00	PER00	GND	PET00	PET00	GND	PER01	PER01	GND	GND	GND	GND	PER02#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PET01	PET01	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND

Figure 105a. Type 1113 Module-side BGA Ballmap (Top View)

In Figure 111 replace text and change color to dark green in cells:

H15: PLN#**RFU**

K15: PLA\_S3#**RFU**>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	R2Q_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3V PWR_1	3.3V PWR_1	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3V PWR_1	3.3V PWR_1	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PETp0	SATA-A- / PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		1.2V PWR_3	1.2V PWR_3	GND	GND	1.2V PWR_3	1.2V PWR_3		GND	GND	DNU	DNU	DNU
H				SATA-B+ / PERp0	SATA-B- / PERn0		1.2V PWR_3	1.2V PWR_3	GND	GND	1.2V PWR_3	1.2V PWR_3		RFU	RFU			
J	GND	GND	GND	GND	GND		1.2V PWR_3	1.2V PWR_3	GND	GND	1.2V PWR_3	1.2V PWR_3		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		1.8V PWR_2	1.8V PWR_2	GND	GND	1.8V PWR_2	1.8V PWR_2		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PERp2	PERn2		1.8V PWR_2	1.8V PWR_2	GND	GND	1.8V PWR_2	1.8V PWR_2		RFU	RFU			
U	GND	GND	GND	GND	GND		1.8V PWR_2	1.8V PWR_2	GND	GND	1.8V PWR_2	1.8V PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED_1# / DAS	RFU	3.3V PWR_1	3.3V PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	3.3V PWR_1	3.3V PWR_1	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	R2Q_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

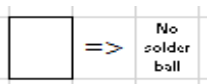


Figure 111. Type 1620 BGA Socket Map **Pinout** On Platform (Top View)

<Editor's Note: In Figure 112 replace text and change color to dark green in cells (using Type 1620 naming grid):

H15: PLN#RFU

K15: PLA\_S3#RFU>

Type 2028			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
Type 2028			Type 2024			Type 1620			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24			
A			DNV	DNV																														DNV	DNV
B	A		DNV					DNV	DNV	DNV	DNV	DNV																DNV	DNV	DNV	DNV	DNV			DNV
C	B	A						DNV	DNV	DNV																						DNV	DNV	DNV	
D	C	B						DNV	DNV																							DNV	DNV		
E	D	C						DNV																									DNV		
F	E	D	A	DNV				DNV				DNV	DNV		DNV		DNV			DNV		DNV			DNV		DNV	DNV	DNV					DNV	
G	F	E	B						DNV	DNV			DNV		CAL_P			DNV			DNV		DNV			DNV		DNV	DNV	DNV					
H	G	F	C	DNV					DNV			GND	GND	GND	GND	GND	XTAL_OUT	XTAL_IN	DNV	RZQ_1	DNV	DNV	RFU	RFU	GND	DNV	DNV	DNV	DNV			DNV			
J	H	G	D									REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	DNV	DEVSLP	DNV	DNV	DNV	DIAG1	SUSCLK	RFU											
K	J	H	E	DNV				DNV				GND	GND	GND	GND	GND	GND	DEVSLP	DNV	DNV	DNV	PEWAKER	DIAG0	GND	GND	DNV	DNV	DNV					DNV		
L	K	J	F									SATA-A+ /PETp0	SATA-A- /PETn0	GND									PEDET	RFU											
M	L	K	G	DNV				DNV				GND	GND	GND	GND	GND									GND	GND	DNV	DNV	DNV					DNV	
N	M	L	H									SATA-B+ /PERp0	SATA-B- /PERn0	GND												RFU	RFU								
P	N	M	J					DNV				GND	GND	GND	GND	GND										GND	GND	DNV	DNV	DNV				DNV	
R	P	N	K									PETp1	PETn1	GND	GND	GND	GND	GND	GND	GND	GND	RFU	RFU												
T	R	P	L					DNV				GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNV	DNV	JTAG_TRST#				DNV		
U	T	R	M									PERp1	PERn1	GND	GND	GND	RFU	RFU	GND	GND	RFU	RFU		RFU	RFU										
V	U	T	N					DNV				GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNV	JTAG_TCK	JTAG_TMS				DNV		
W	V	U	P									PETp2	PETn2	GND	GND	GND	GND	GND	GND	GND	GND		RFU	RFU											
Y	W	V	R					DNV				GND	GND	GND	GND	GND										GND	DNV	JTAG_TDI	JTAG_TDO					DNV	
AA	Y	W	T									PERp2	PERn2	GND	GND	GND										RFU	RFU								
AB	AA	Y	U	DNV				DNV				GND	GND	GND	GND	GND										GND	GND	DNV	SMB_CLK	SMB_DATA				DNV	
AC	AB	AA	V									PETp3	PETn3	GND	GND	GND										RFU	RFU								
AD	AC	AB	W	DNV				DNV				GND	GND	GND	GND	GND		LED_16/DAS	RFU	DNV	DNV	GND	RFU	RFU	GND	GND	DNV	DNV	ALERT#				DNV		
AE	AD	AC	Y									PERp3	PERn3	GND	GND	GND	DNV	DNV	DNV	DNV	DNV	DNV	GND	DNV	DNV	DNV	DNV	DNV	DNV	DNV					
AF	AE	AD	AA	DNV				DNV				GND	GND	GND	GND	GND		DNV	DNV	DNV	DNV	DNV	DNV	GND	DNV	DNV	DNV	DNV	DNV	DNV	DNV			DNV	
AG	AF	AE	AB						DNV	DNV			DNV		DNV			DNV								DNV		DNV	DNV	DNV					
AH	AG	AF	AC	DNV				DNV				DNV	DNV		DNV			DNV								DNV		DNV	DNV					DNV	
AJ	AH	AG						DNV																										DNV	
AK	AJ	AH						DNV	DNV																									DNV	
AL	AK	AJ						DNV	DNV	DNV																								DNV	
AM	AL			DNV					DNV	DNV	DNV	DNV	DNV																					DNV	
AN				DNV	DNV																														DNV

— — — — —	Type 1620
— — — — —	Type 2024
— — — — —	Type 2228
— — — — —	Type 2828

Figure 112. Type 1620, Type 2024, Type 2228, Type 2828 BGA  
Pinout On Platform Socket Map On Platform (Top View)

<Editor's Note: In Figure 1 replace text and change color to dark green in cells:

C10: ~~PLN#~~RFU

D10: ~~PLA S3#~~RFU>

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND
B	GND	GND	GND	REG_01	REG_02	REG_03			GND			GND			GND	WP_L	SPL_CLK	SPL_CS_L	GND	GND
C	GND	GND	GND	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_DATA	ALERT#	DIAG0	JTAG_TMS	JTAG_TDI	SPL_MOSI	SPL_MISO	GND	GND	GND
D		PWR_2	PWR_2	DNU	DNU	RFU	RFU	RFU	RFU	RFU	SMB_CLK	DIAG1	JTAG_TRST#	JTAG_TDO	JTAG_TCK	RFU	SPL_18	PWR_2	PWR_2	
E	GND	PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	GND
F		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	
H	GND	PWR_1	PWR_1	HSB	HSB	HSB	HSB								HSB	HSB	GND	PWR_1	PWR_1	GND
J		PWR_1	PWR_1	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	PWR_1	PWR_1	
K		GND	PWR_1	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_1	GND	
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND
M	GND	GND	PWR_3	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	PWR_3	GND	GND
N		PWR_3	PWR_3	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	PWR_3	PWR_3	
P		PWR_3	PWR_3	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	PWR_3	PWR_3	
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND
T		PWR_2	PWR_2	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
U		PWR_2	PWR_2	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	PWR_2	PWR_2	
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND
W		SUSCLK	CLKREQ#	PERST#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	CAL_P	XTAL_OUT	XTAL_IN	
Y	GND	LED_1#	GND	GND	GND	GND	PETp0	PETn0	GND	PERp0	PERn0	GND	PETp1	PETn1	GND	GND	GND	GND	PEWAKE#	GND
AA	GND	GND	GND	REFCLKp	REFCLKn	GND			GND			GND			GND	PERp1	PERn1	GND	GND	GND
AB	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND

Figure 1. Type 1113 BGA Socket Map On Platform (Top View)